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(71) Applicant: **SONY CORPORATION**
Tokyo 141 (JP)

(72) Inventors:
- **Horiguchi, Mari**
  Shinagawa-ku, Tokyo (JP)
- **Yanagihara, Naofumi**
  Shinagawa-ku, Tokyo (JP)

(74) Representative:
Robinson, Nigel Alexander Julian et al
D. Young & Co.,
21 New Fetter Lane
London EC4A 1DA (GB)

(54) Apparatus and method for transmitting data

(57) DVD reproducing apparatus (902) which transmits variable-bit rate data on a digital serial bus (901) having a predetermined transmission rate. The DVD reproducing apparatus reproduces data from a record medium (1) in accordance with a control signal to produce variable rate data. The peak data rate of the variable rate data is detected (8), a rate of transmission of the variable rate data is established in accordance with the detected peak data rate, and the variable rate data is transmitted in accordance with the established transmission rate. The DVD reproducing apparatus includes an MPEG decoder (6) which MPEG decodes the reproduced data and which generates the control signal in accordance with amounts of data stored within various buffers (64,65), such control signal being utilized to control the reproduction of the data from the record medium. A receiver (220,500), e.g., a digital television (200), having an MPEG decoder (9) therein receives the transmitted data and MPEG decodes the data, but such MPEG decoder does not generate a control signal similar to the previously generated control signal in order to prevent underflow/overflow of the memories therein. In another embodiment, the DVD reproducing apparatus does not include therein an MPEG decoder, but the receiving device's MPEG decoder, unlike the first mentioned embodiment, generates a control signal that is transmitted back to the DVD reproducing apparatus in order to prevent underflow/overflow of the memories within the receiving device's MPEG decoder.

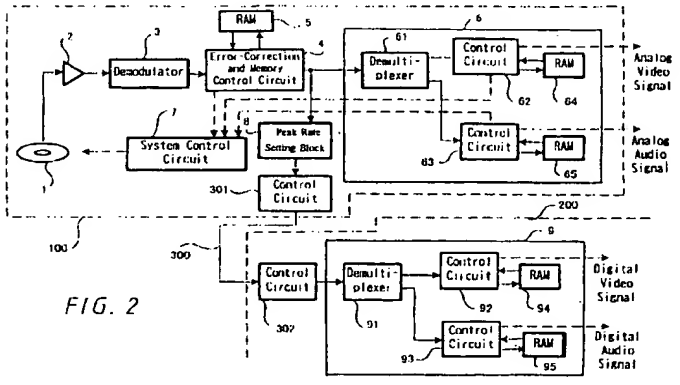

FIG. 2

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Description

The present invention relates to an apparatus and a method for transmitting data and, more particularly, but not exclusively, to an apparatus and a method for transmitting variable-bit rate data on a digitial serial bus having a predetermined transmission rate.

As is known, various types of digital video-audio equipment, for example, DVD reproducing devices, digital VTRs, digital televisions, etc., are currently available for consumer use. Several such devices reproduce or receive digital video/audio signals, convert those signals into analog signals, and supply the analog signals to analog-type video/audio equipment. It is also generally desirable to supply from such equipment digital video/audio signals to, for example, a personal computer, a digital television receiver, or other type of digital device.

The communication system IEEE-1394 is a digital serial bus which has been proposed as a means for transmitting such digital video/audio signals between digital devices. Referring to Fig. 1 of the drawings, an exemplary block diagram of an IEEE-1394 system that includes an IEEE-1394 bus 901 and various digital devices 902-907 is shown. In the exemplary block diagram, the IEEE-1394 bus is coupled between a DVD reproducing apparatus 902, a digital VCR 903, a digital broadcasting receiver 904, a digital television receiver 905, a digital television receiver 906 and a personal computer 907. As shown, digital video/audio data is supplied from DVD reproducing apparatus 902 via the IEEE-1394 bus to digital television receiver 906, and digital video/audio data supplied from digital broadcasting 904 is supplied via bus 901 to digital television receiver 905. Given an IEEE-1394 bus with a transmission rate of, for example, 100 Mbps, and video/audio data is organized into "units" of data, then in accordance with IEEE-1394 standard, 4915 units of data can be transmitted during each 125 μsec transmission cycle of the bus. In accordance with this standard, the number of units transmitted corresponds to the bit rate of the signal to be transmitted. For example, to realize a communication speed of approximately 10 Mbps, which corresponds to the mean bit rate of a typical video signal, then approximately 1200 units are needed. However, to realize a communication speed of approximately 2 Mbps, which is the mean bit rate of an audio signal, then approximately 704 units are needed.

One limitation of the above discussed IEEE-1394 standard is that signals are transmitted only after their transmission rate (i.e., bit rate) is determined. However, DVD reproducing devices that employ MPEG encoders/decoders reproduce digital video/audio data at a variable rate and, thus, an IEEE 1394-bus previously has been unable to transmit variable rate data reproduced from such devices.

Therefore, it is an object of the present invention to provide an apparatus and a method for transmitting digital video/audio data which address the shortcomings of the above described system.

Various aspects of the present invention are set out in the accompanying claims.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a system employing an IEEE-1394 digital serial bus;

Fig. 2 is a block diagram of a data transmission apparatus in accordance with one embodiment of the present invention;

Fig. 3 is a block diagram of a data transmission apparatus in accordance with another embodiment of the present invention;

Fig. 4 is a simplified block diagram of the device shown in Fig. 2;

Fig. 5 is a simplified block diagram of the device shown in Fig. 3;

Fig. 6 is a block diagram of control circuits 301 and 302 in accordance with one embodiment of the present invention;

Fig. 7 schematically illustrates the data structure of an Iso packet; and

Fig. 8 is a schematic illustration of the transmission bandwidth of a digital serial bus that is transmitting data in accordance with the present invention.

Figs. 2 and 3 illustrate different exemplary embodiments of the data transmission apparatus of the present invention, wherein Fig. 2 illustrates a DVD reproducing apparatus 100 that includes an MPEG decoder 6, and Fig. 3 illustrates a DVD reproducing apparatus 100 that does not include an MPEG decoder. As will be discussed, DVD reproducing apparatus 100 shown in both Figs. 2 and 3 are coupled via an IEEE-1394 digital serial bus 300 to an MPEG decoder 9, included in, for example, a digital television receiver.

Referring first to the embodiment of the present invention shown in Fig. 2, DVD reproducing apparatus 100 is operable to reproduce digital video/audio data from a digital video disk, decode the reproduced data in MPEG decoder 6, and supply the decoded data as respective analog video and audio signals. The analog video and audio signals may be supplied to, for example, an analog television receiver, an analog recording device, etc. DVD reproducing apparatus 100 further is operable to transmit the reproduced digital video/audio data via bus 300 to an external MPEG decoder 9 which decodes the transmitted signal and supplies digital video and audio signals as an output.

DVD reproducing apparatus 100 of the present invention reproduces digital video/audio data from a digital video disk in a reproducing device 1 which supplies the reproduced data via an amplifier circuit 2 to a demodulator 3 which demodulates the reproduced signal. The demodulated signal is supplied to an error correc-

tion and memory control circuit 4 which stores the supplied signal in a random access memory 5 and corrects errors in the stored signal in a known manner. The error corrected signal is supplied to MPEG decoder 6 which includes therein a demultiplexer 61, control circuits 62 and 63, and random access memories 64 and 65. The digital signal is supplied to demultiplexer 61 which demultiplexes the signal into its respective video and audio components. The video signal is stored via control circuit 62 in memory 64, and the audio signal is stored via control circuit 63 in memory 65. Control circuits 62 and 63 decode the respective stored video and audio signals in a known manner and the decoded video and audio signals are supplied as, for example, analog video and audio output signals (after digital to analog conversion).

In addition to decoding the stored video and audio signals, control circuits 62 and 63 supply to a system control circuit 7 respective control signals that identify the storage states of the respective memories 64, 65. Similarly, memory control circuit 4 supplies to system control circuit 7 a control signal that identifies the storage state of memory 5. These control signals are sometimes identified as memory occupation data and generally identify how much data is stored in the respective memories. System control circuit 7, in response to the supplied control signals, controls the reproduction of the digital video/audio data by the reproducing device 1 so as to, *inter alia,* prevent the underflow and/or overflow of the memories.

In accordance with this embodiment of the present invention, DVD reproducing apparatus 100 includes a peak rate setting block 8 which sets the peak rate of the reproduced data for purposes of transmission of the variable-rate data on bus 300 (to be further discussed). DVD reproducing apparatus 100 further includes a control circuit 301 which transmits the error corrected digital signal output by circuit 4 on bus 300 in accordance with the IEEE-1394 standard. In addition to supplying the error corrected digital video/audio signal to MPEG decoder 6, error correction and memory control circuit 4 supplies the error corrected digital video/audio signal to peak rate setting block 8.

As previously mentioned, the mean bit rate of a typical video signal is 10 Mbps, and the mean bit rate of a typical audio signal is 2Mbps. In accordance with this embodiment of the present invention, peak rate setting block 8 sets the peak rates of the video and audio signals to twice their respective mean bit rates, that is, 20 Mbps and 4 Mbps, respectively. Control circuit 301 calculates from the supplied set peak rate the number of units that are required, and in accordance with the IEEE-1394 standard to provide a total transmission speed of, for example, 100 Mbps on the digital serial bus, 2400 units and 1408 units are required to transmit the video and audio signals, respectively. The transmission band necessary then is said to be "secured" in accordance with the standard.

Referring to Fig. 8, prior to each 125 μsec transmission cycle of the IEEE-1394 bus 300 during which the video and audio signals are transmitted, the required transmission band is secured by control circuit 301, such transmission band being represented by the dashed rectangular portion in each cycle in Fig. 8. That is, the regions surrounded by the dashed rectangular portions are said to be "secured" for the data that is to be transmitted by DVD reproducing apparatus 100 of the present invention. The hatched portion of each secured rectangular portion of each cycle represents that portion of the secured transmission band that is actually utilized, i.e., the hatched portions represent the variable rate data itself. The unsecured transmission band corresponds to those regions beyond the dashed rectangular portions and are usable by other devices, for example, digital VCR 903 shown in Fig. 1.

Control circuit 301 secures the necessary transmission band and subsequently transmits the digital signal (video and audio) supplied from error correction and memory control circuit 4 on the secured transmission band of bus 300. The digital signal is transmitted to a control circuit 302 which operates to control the bus communication in accordance with the IEEE-1394 standard, which control circuit 302 being included in, for example, a digital television receiver 200 that includes an MPEG decoder 9. Therefore, and in accordance with the present invention, variable bit rate data reproduced by DVD reproducing apparatus 100 is transmitted on a digital serial bus in accordance with the IEEE-1394 standard.

The transmitted video/audio data is supplied from control circuit 302 to MPEG decoder 9 which has a structure similar to that of MPEG decoder 6, but control circuits 92, 93 do not produce control signals that identify the storage state of memories 94, 95. The digital video/audio signal is supplied to a demultiplexer 91 which demultiplexes the signal into its respective video and audio components which are then stored via control circuits 92 and 93 in random access memories 94 and 95, respectively. The respective digital and audio signals are decoded by control circuits 92 and 93 and the decoded video and audio signals are supplied as, for example, respective digital video and audio signals.

As previously mentioned, control circuits 92 and 93 do not generate control signals that identify the storage states of memories 94 and 95. DVD reproducing apparatus 100 operates to MPEG decode the reproduced signal in MPEG decoder 6 and simultaneously transmit the reproduced signal on bus 300. Since MPEG decoder 9 is equivalent to MPEG decoder 6, and since control circuits 62 and 63 generate respective control signals representing the storage states of memories 64 and 65, which in turn controls the reproduction of the data from the digital video disk, it is unnecessary for control circuits 92 and 93 to generate controls signals that identify the respective storage states of memories 94 and 95. In other words, the storage states of memories 64 and 65 should be substantially equivalent to the storage states

of memories 94 and 95, respectively and, thus, proper control of the reproduction of the digital video/audio data from the digital video disk is provided solely by MPEG decoder 6.

As previously mentioned, MPEG decoder 6 may supply as outputs respective analog video and audio signals and such signals may be supplied on an analog signal line 400 to an analog television receiver 500, such as shown in Fig. 4.

In accordance with this embodiment of the present invention, as discussed above, the storage states of memories 64 and 65 are detected and the reproduction operation of DVD reproducing apparatus 100 is controlled in accordance with such storage states thus preventing underflow and overflow of memories 64 and 65. By the use of MPEG decoder 6, a separate MPEG decoder 9, that is coupled to DVD reproducing apparatus 100 via digital serial bus 300, does not need to determine whether an underflow or overflow condition of memories 94 and 95 exists. Furthermore, by detecting the peak rate of the supplied digital video/audio signal periodically in peak rate setting block 8, variable rate data may be transmitted on a digital serial bus in accordance with the IEEE-1394 standard, even when such standard requires that the transmitted bit rate be known.

Referring next to Fig. 3 of the drawings, a block diagram of apparatus for transmitting digital video and audio data in accordance with another embodiment of the present invention is shown. Fig. 5 also illustrates the present embodiment, wherein DVD reproducing apparatus 100 is coupled to a digital television 200 including therein a display unit and MPEG decoder 9. Referring back to Fig. 3, DVD reproducing apparatus 100 includes a DVD reproducing device 1, an amplifier 2, a demodulator 3, an error correction and memory control circuit 4, a random access memory 5, a peak rate setting block 8, a system control circuit 7 and a control circuit 301 and thus is similar to DVD reproducing apparatus 100 shown in Fig. 2, except the DVD reproducing device of the present embodiment does not include an internal MPEG decoder 6. In the present embodiment, circuits 1-5 operate in a manner identical to that of circuits 1-5 shown in Fig. 2, wherein digital video/audio data is reproduced from a digital video disk, demodulated, stored in memory 5, error corrected in circuit 4 and supplied as an error corrected digital video/audio signal to control circuit 301 via peak rate setting block 8. Peak rate setting block 8 operates in the same manner as that described above with respect to the embodiment shown in Fig. 2 and, therefore, further-description thereof is omitted herein. Also, like the embodiment shown in Fig. 2, control circuit 301 shown in Fig. 3 secures the necessary bandwidth in accordance with the peak rate detected by peak rate setting block 8 and transmits on bus 300 the error corrected digital video/audio signal in accordance with the IEEE-1394 standard, all as previously discussed.

The transmitted digital video/audio signal is supplied to a control circuit 302 included in digital television receiver 200 which supplies the received signal to an MPEG decoder 9 which includes therein a demultiplexer 91, control circuits 92 and 93, and memories 94 and 95. Demultiplexer 91 demultiplexes the transmitted signal into its respective video and audio components, and stores the video data via control circuit 92 in memory 94 and stores the audio data via control circuit 93 in memory 95. Control circuits 92 and 93 MPEG decode the respective video and audio data to produce respective digital video and audio signals.

In accordance with this embodiment of the present invention, control circuits 92 and 93 detect the storage states (conditions) of memories 94 and 95, respectively (like control circuits 62 and 63 in Fig. 2), and generate therefrom respective control signals that are supplied to control circuit 302. Also in accordance with this embodiment of the present invention, the control signals supplied from control circuits 92 and 93 to control circuit 302 are transmitted from control circuit 302 on digital serial bus 300 to control circuit 301 in DVD reproducing apparatus 100.

In accordance with the IEEE-1394 standard, control circuits 301 and 302 each have a block structure as shown in Fig. 6, wherein each control circuit includes an Iso packet transmitting and receiving block 310, a bus control block 311, an information signal processing block 312 and a plug control register 313 located within bus control block 311. Iso packet transmitting and receiving block 310 performs isochronous communication for transmitting the video signal data and audio signal data, and bus control block 311 performs asynchronous communication for transmitting control signals. Data is transmitted between the Iso packet transmitting and receiving block 310 and information signal processing block 312 within each control circuit 301 and 302. In accordance with the IEEE-1394 standard, the Iso packet that is transmitted between control circuit 301 and 302 has the data structure as shown in Fig. 7.

Referring to Fig. 7, each Iso packet is formed from "quadlets" of data, each quadlet consisting of four bytes of information. The Iso packet includes a header, which includes therein the data length that is provided in the so-called first quadlet. The Iso packet header further includes in the second quadlet cyclic redundancy check (CRC) codes for the information of the fist quadlet. As shown, the packet header is comprised of the first and second quadlets, such packet header being transmitted at the beginning of packet transmission. A data field follows the packet header, and the cyclic redundancy check codes for the data field follows that data field.

Bus control block 311 of each control circuit 301 and 302 receives from the respective information processing block 312 the control signals that identify the storage states of memories 94 and 95. Such information is transmitted from one control circuit to another control circuit utilizing asynchronous communication. Typically, control circuit 302 transmits such control signals asynchronously to control circuit 301 which subsequently sup-

plies the transmitted control signals to system control circuit 7. As previously mentioned, bus control block 311 of each control circuit 301, 302 includes a respective plug control register 313. Plug control register 313 sets values stored therein in accordance with the transmitted information, for example, the transmitted signals, and the various information generated by the particular equipment utilized, and Iso packet transmitting and receiving block 310 of the respective control circuit 301, 302 is controlled in accordance with the values stored in plug control register 313.

Finally, the control signals transmitted to system control circuit 7 from control 301 operate to control the reproducing operation of DVD reproducing circuit 1 in order to prevent underflow and overflow of memories 94 and 95.

Like the first embodiment previously discussed with reference to Fig. 2, the embodiment of Fig. 3 is operable to transmit variable rate data across a transmission line, for example, IEEE-1394 bus 300, which has a predetermined rate of transmission. Referring again to Fig. 8, the transmission band is secured prior to the transmission of the digital video/audio data and, as previously discussed, the hatched portion of the secured bandwidth of each cycle represents the variable rate data itself supplied by DVD reproducing apparatus 100, and the unsecured transmission band corresponds to those regions beyond the dashed rectangular portions and are usable by other devices.

At least preferred embodiments of the invention provide:

an apparatus and a method which is operable to transmit variable rate digital video/audio data in accordance with the IEEE-1394 standard;

an apparatus and a method for detecting a peak data rate of variable rate data to be transmitted, establishing a rate of transmission of the variable rate data in accordance with the detected peak data rate, and transmitting in accordance with the established transmission rate the variable rate data on a transmission line that requires the transmission rate to be predetermined;

a system in which a bandwidth of the transmission line that is required to transmit the variable rate data having the detected peak data rate is secured ;

a system in which the reproducing of a signal from a record medium to produce the variable rate signal is controlled in accordance with a control signal, the variable rate signal is processed (e.g., by an MPEG decoder), the control signal is generated in accordance with a condition of processing of the produced variable rate signal, and the variable rate signal is transmitted on the transmission line;

a system in which the transmitted variable rate signal is received and processed in a similar manner as that of the produced variable rate signal (e.g., by a second MPEG decoder), but such second processing does not generate a control signal (similar to the earlier generated control signal) that represents a condition of the second processing; and

a system in which the transmitted variable rate signal is received by a receiver (e.g., a digital television), the received transmitted variable rate signal is processed, the control signal is generated in accordance with a condition of processing of the received transmitted variable rate signal, and the generated control signal is transmitted back to the transmitting side, wherein the received transmitted control signal is utilized to control the reproducing of a signal from the record medium.

While the present invention has been particularly shown and described in conjunction with preferred embodiments thereof, it will be readily appreciated by those of ordinary skill in the art that various changes may be made without departing from the scope of the invention. For example, the present invention, although described with reference to the IEEE-1394 standard and the use of MPEG decoders, is not limited to this standard and/or the use of MPEG decoders, but may be applied to other standards and/or other types of coders/decoders that produce/decode variable-rate data.

Therefore, it is intended that the appended claims be interpreted as including the embodiments described herein, the alternatives mentioned above, and all equivalents thereto.

Claims

1. Apparatus for transmitting variable rate data on a transmission line requiring a predetermined rate, comprising:

   detection means for detecting a peak data rate of variable rate data to be transmitted;
   means for establishing a transmission rate of said variable rate data in accordance with the detected peak data rate; and
   means for transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

2. The apparatus of claim 1, wherein said means for establishing includes means for securing a bandwidth of said transmission line required to transmit said variable rate data having said detected peak data rate.

3. The apparatus of claim 2, wherein said transmission line has a plurality of cycles, and said means for securing a bandwidth secures the same bandwidth for each cycle of said transmission line.

4. The apparatus of claim 1, further comprising:

means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
processing means for processing the produced variable rate signal, said processing means including means for generating said control signal in accordance with a condition of processing of the produced variable rate signal by said processing means.

5. The apparatus of claim 4, wherein said processing means is operable to MPEG decode the produced variable rate signal.

6. The apparatus of claim 4, wherein said processing means includes buffering means for buffering the produced variable rate signal, and said means for generating said control signal generates said control signal representing a state of said buffering means.

7. The apparatus of claim 4, further comprising reception means for receiving the variable rate signal transmitted on said transmission line, said reception means including reception processing means for processing the received transmitted variable rate signal in a similar manner as said processing means processes the produced variable rate signal, said reception processing means not generating a control signal that controls the reproduction of the signal from the record medium.

8. The apparatus of claim 7, wherein said processing means and said reception processing means are both MPEG decoders.

9. The apparatus of claim 1, further comprising:

means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce said variable rate signal; and
reception means for receiving the variable rate signal transmitted on said transmission line, said reception means including reception processing means for processing the received transmitted variable rate signal, said reception processing means including means for generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal by said reception processing means, said reception means further including reception transmitting means for transmitting the generated control signal to said transmitting means;
wherein said transmitting means is operable to receive the transmitted control signal and to supply the received transmitted control signal to said means for controlling.

10. The apparatus of claim 9, wherein said reception processing means includes buffering means for buffering the received transmitted variable rate signal, and said means for generating said control signal generates said control signal representing a state of said buffering means.

11. The apparatus of claim 10, wherein said reception processing means is an MPEG decoder.

12. Apparatus for transmitting variable rate data on a transmission line requiring a predetermined rate, comprising:

a peak bit rate detector for detecting a peak data rate of variable rate data to be transmitted; and
a bus controller for establishing a transmission rate of said variable rate data in accordance with the detected peak data rate, and for transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

13. The apparatus of claim 12, wherein said bus controller is operable to secure a bandwidth of said transmission line required to transmit said variable rate data having said detected peak data rate.

14. The apparatus of claim 13, wherein said transmission line has a plurality of cycles, and said bus controller secures the same bandwidth for each cycle of said transmission line.

15. The apparatus of claim 12, further comprising:

a reproducing device controller for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
a processor for processing the produced variable rate signal, said processor being operable to generate said control signal in accordance with a condition of processing of the produced variable rate signal by said processor; and
a transmission line controller for transmitting the variable rate signal on said transmission line.

16. The apparatus of claim 15, wherein said processor is an MPEG decoder.

17. The apparatus of claim 15, wherein said processor includes a data buffer for buffering the produced variable rate signal, and said control signal generated by said processor represents a state of said

data buffer.

18. The apparatus of claim 15, further comprising a receiver for receiving the variable rate signal transmitted on said transmission line, said receiver including a reception processor for processing the received transmitted variable rate signal in a similar manner as said processor processes the produced variable rate signal, said reception processor not generating a control signal that controls the reproduction of the signal from the record medium.

19. The apparatus of claim 18, wherein said processor and said reception processor are both MPEG decoders.

20. The apparatus of claim 12, further comprising:

a reproducing device controller for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
a transmitter for transmitting the variable rate signal on said transmission line; and
a receiver for receiving the variable rate signal transmitted on said transmission line, said receiver including a reception processor for processing the received transmitted variable rate signal, said reception processor generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal by said reception processor, said receiver further being operable to transmit the generated control signal to said transmitter;
wherein said transmitter is operable to receive the transmitted control signal and to supply the received transmitted control signal to said reproducing device controller.

21. The apparatus of claim 20, wherein said reception processor includes a data buffer for buffering the received transmitted variable rate signal, and said control signal generated by said reception processor represents a state of said data buffer.

22. The apparatus of claim 21, wherein said reception processor is an MPEG decoder.

23. Method of transmitting variable rate data on a transmission line requiring a predetermined rate, comprising the steps of:

detecting a peak data rate of variable rate data to be transmitted;
establishing a transmission rate of said variable rate data in accordance with the detected peak data rate; and
transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

24. The method of claim 23, wherein said step of establishing is carried out by securing a bandwidth of said transmission line required to transmit said variable rate data having said detected peak data rate.

25. The method of claim 24, wherein said transmission line has a plurality of cycles, and the same bandwidth is secured for each cycle of said transmission line.

26. The method of claim 23, further comprising the steps of:

controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
processing the produced variable rate signal;
generating said control signal in accordance with a condition of processing of the produced variable rate signal; and
transmitting the variable rate signal on said transmission line.

27. The method of claim 26, wherein said processing step is carried out by MPEG decoding the produced variable rate signal.

28. The method of claim 26, wherein said processing step includes the step of buffering the produced variable rate signal in a buffer, and said generated control signal represents a state of said buffer.

29. The method of claim 26, further comprising the steps of receiving the variable rate signal transmitted on said transmission line, and processing the received transmitted variable rate signal in a similar manner as said variable rate signal is processed in said first processing step, wherein a control signal representing a condition of processing of the received transmitted variable rate signal similar to the previously generated control signal is not generated.

30. The method of claim 29, wherein said first and second processing steps are carried by respective MPEG decoders.

31. The method of claim 23, further comprising the steps of:

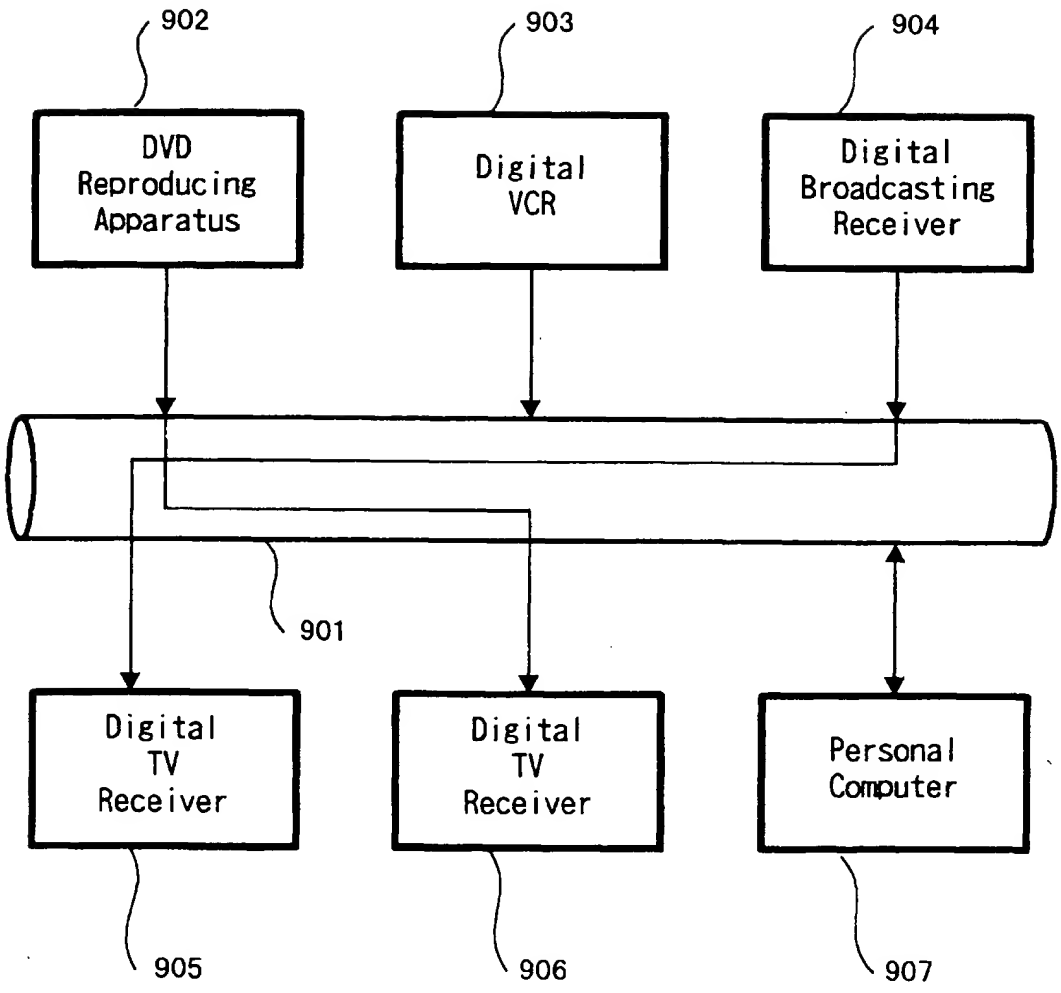
controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
transmitting from a transmission side the vari-

able rate signal on said transmission line;
receiving the variable rate signal transmitted on said transmission line;
processing the received transmitted variable rate signal;
generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal;
transmitting the generated control signal on said transmission line; and
receiving at said transmission side the transmitted control signal;
wherein the received transmitted control signal is utilized to control the reproducing by said controlling step.

32. The method of claim 31, wherein said processing step includes the step of buffering the received transmitted variable rate signal in a buffer, and the generated control signal represents a state of said buffer.

33. The method of claim 32, wherein said processing step is carried out by an MPEG decoder.

FIG. 1


902
903
904
DVD Reproducing Apparatus
Digital VCR
Digital Broadcasting Receiver
901
Digital TV Receiver
Digital TV Receiver
Personal Computer
905
906
907

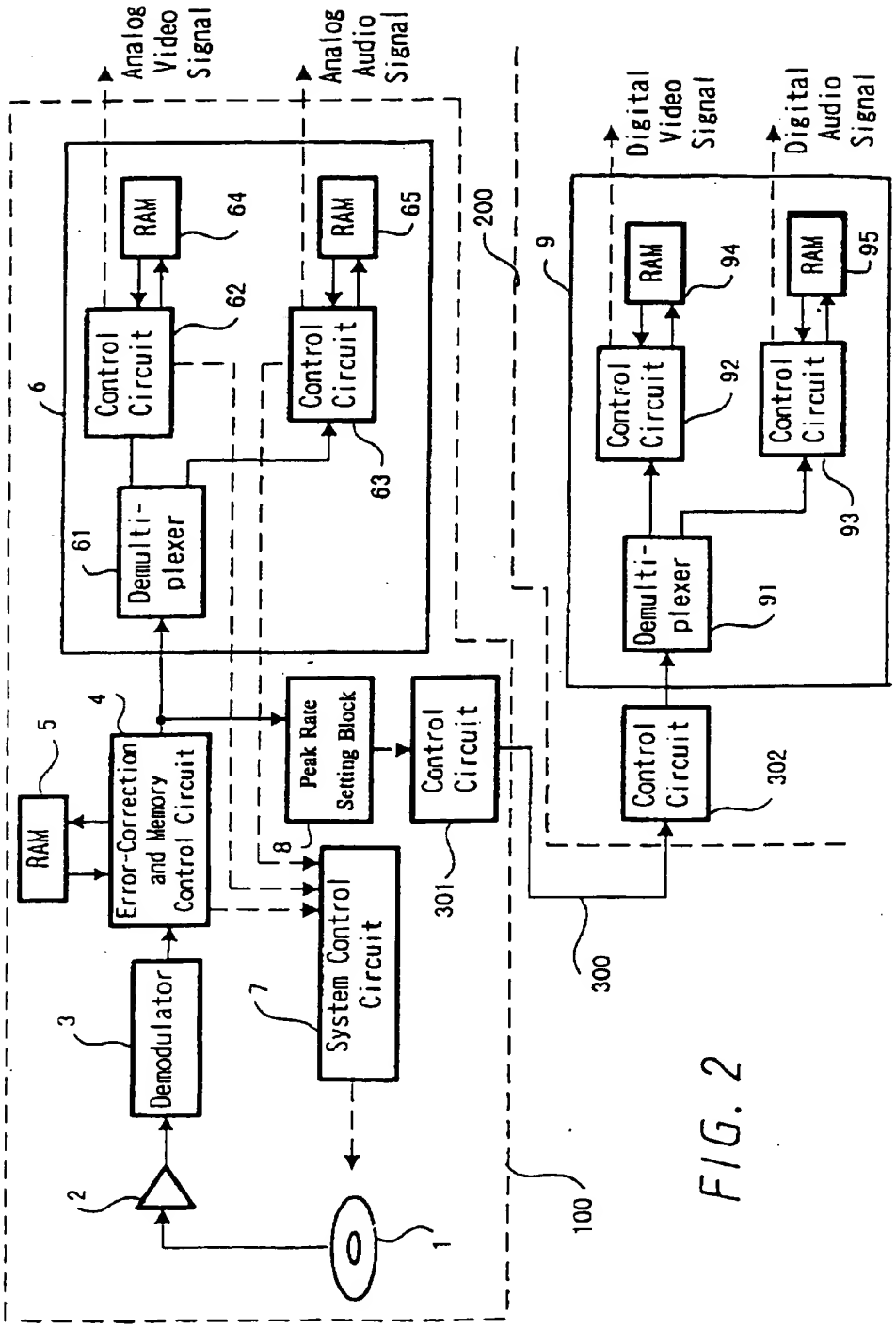

Analog Video Signal
Analog Audio Signal
Digital Video Signal
Digital Audio Signal
RAM
Control Circuit
Demulti-plexer
Error-Correction and Memory Control Circuit
Peak Rate Setting Block
System Control Circuit
Demodulator
100
200
300
301
302

FIG. 2

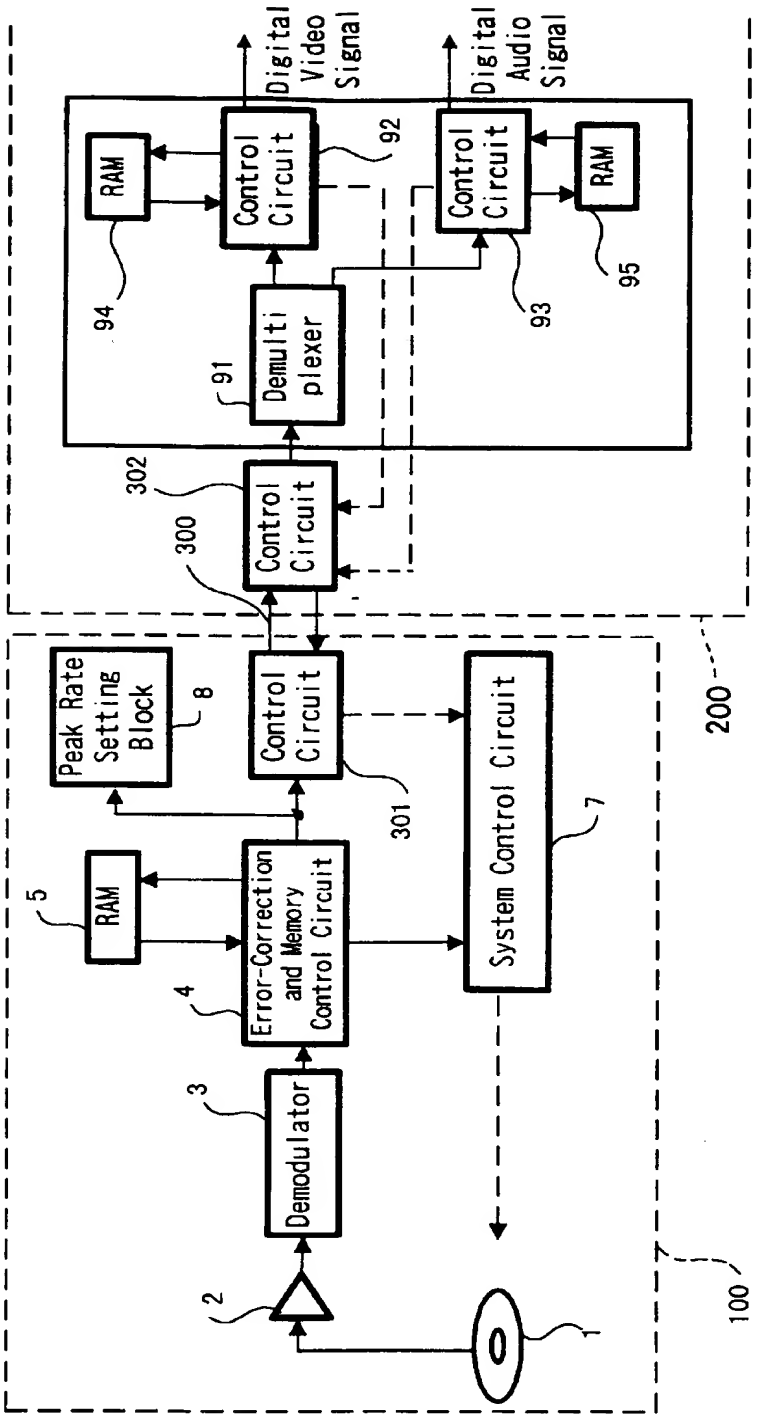

Digital Video Signal
Digital Audio Signal
Control Circuit
92
RAM
94
Demulti plexer
91
Control Circuit
93
RAM
95
302
Control Circuit
300
200
Peak Rate Setting Block
8
Control Circuit
301
System Control Circuit
7
RAM
5
Error-Correction and Memory Control Circuit
4
Demodulator
3
2
1
100

FIG. 3

FIG. 4

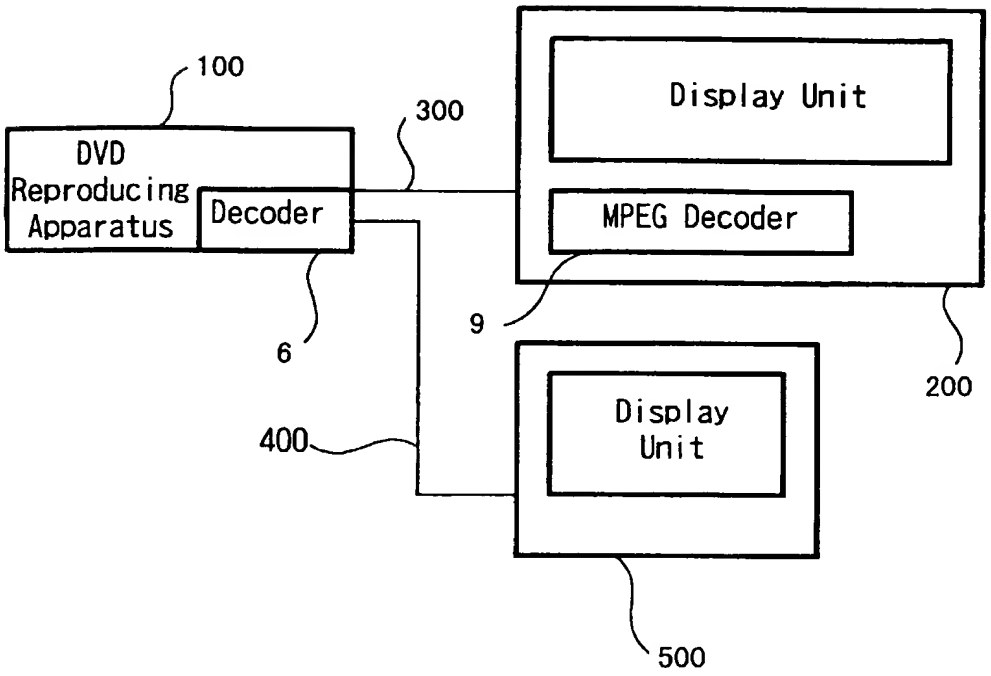

100
DVD
Reproducing
Apparatus
Decoder
300
Display Unit
MPEG Decoder
6
9
200
400
Display
Unit
500

FIG. 5

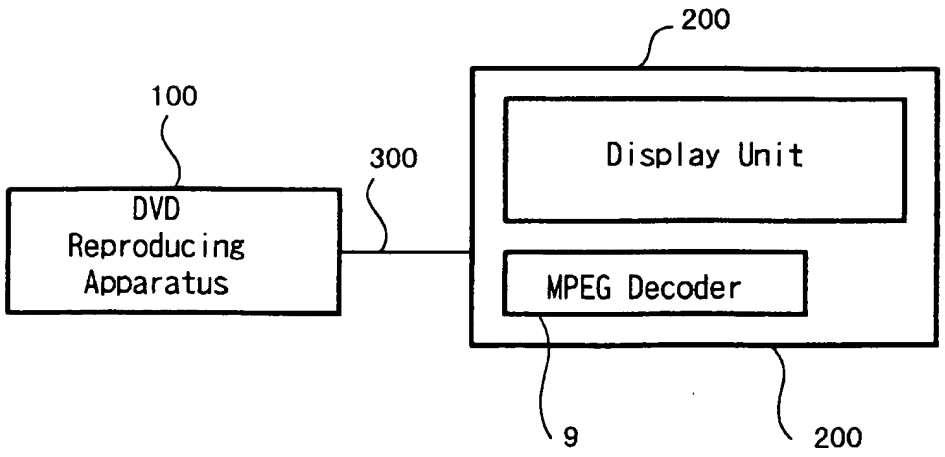

200
100
300
Display Unit
DVD
Reproducing
Apparatus
MPEG Decoder
9
200

FIG. 6

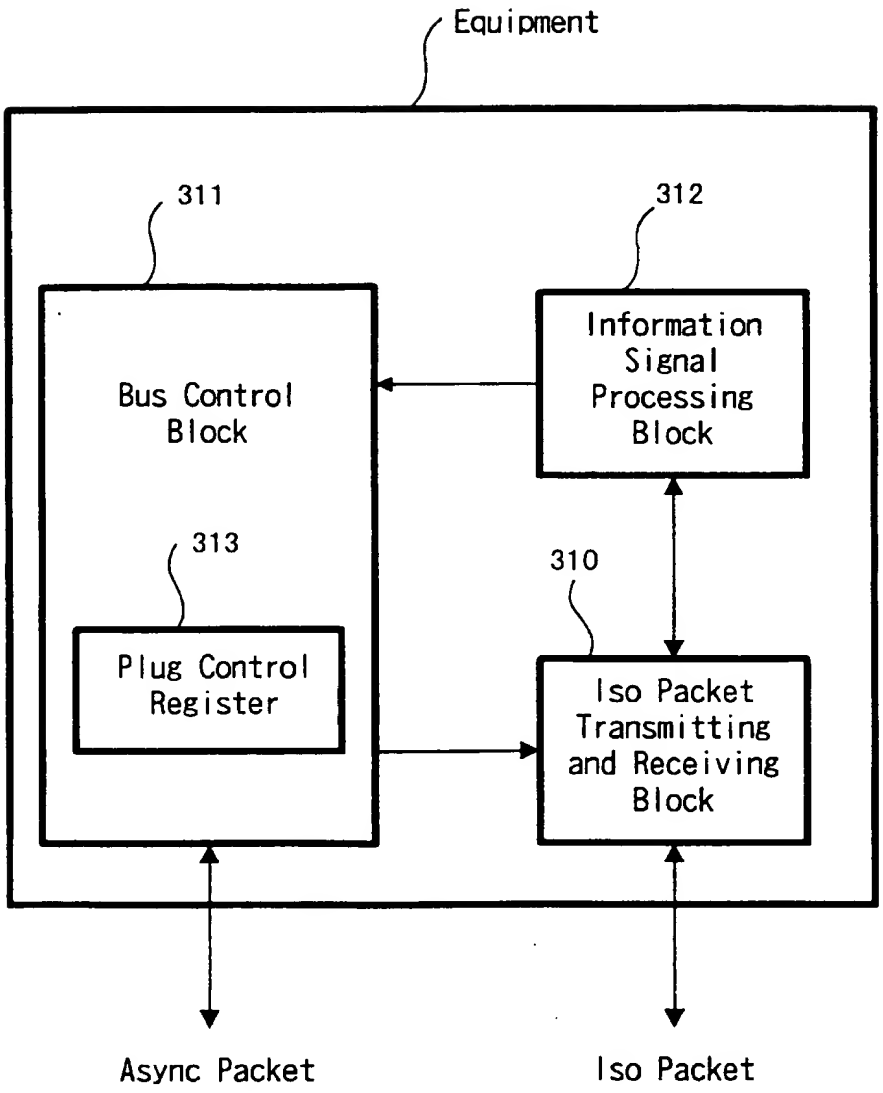

Equipment
311
312
Bus Control Block
Information Signal Processing Block
313
310
Plug Control Register
Iso Packet Transmitting and Receiving Block
Async Packet
Iso Packet

FIG. 7

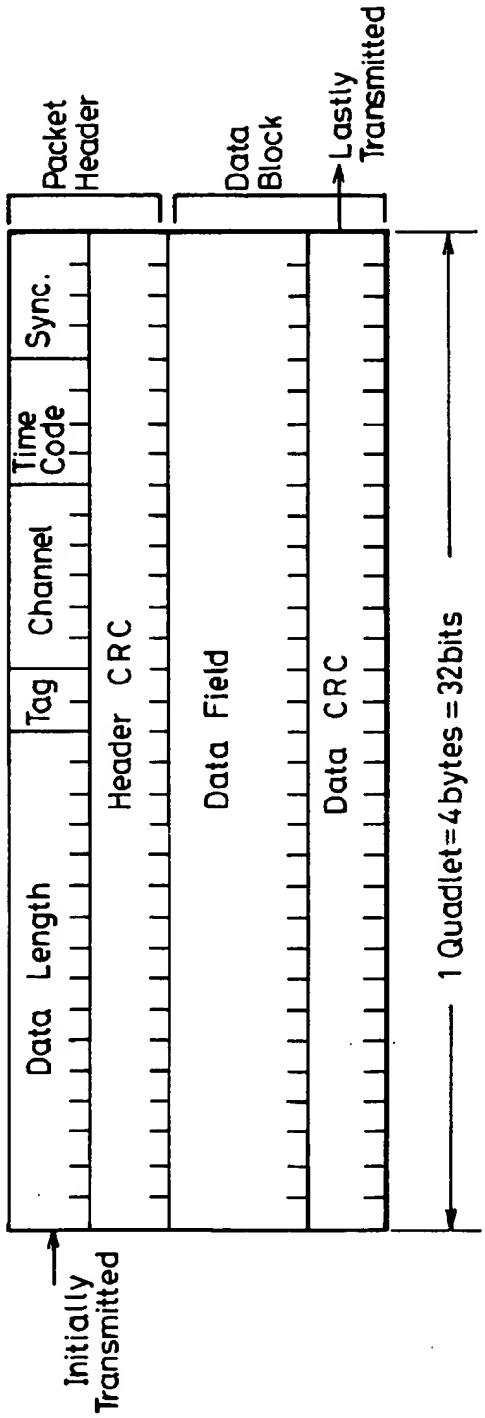
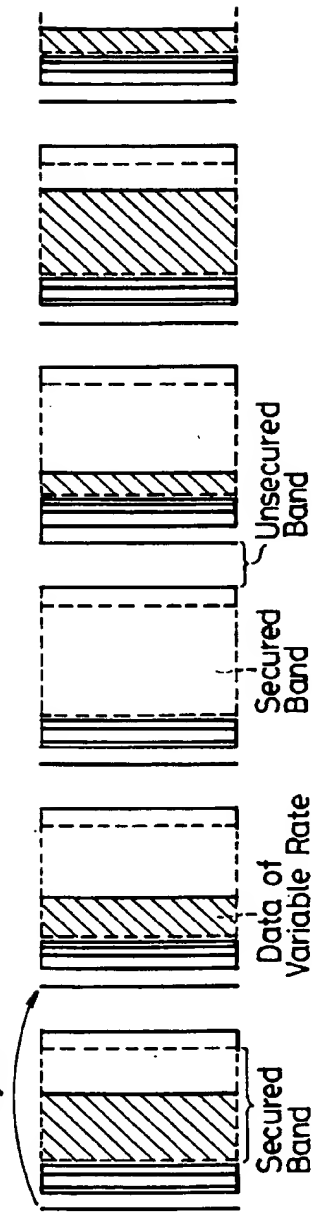

Packet Header
Data Block
Lastly Transmitted
Data Length
Tag
Channel
Time Code
Sync.
Header CRC
Data Field
Data CRC
1 Quadlet=4 bytes=32bits
Initially Transmitted

FIG. 8


1cycle
Secured Band
Data of Variable Rate
Secured Band
Unsecured Band